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10/623,028	07/17/2003	Derek Shaeffer	15436.928.4.1	8766

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EXAMINER	
CHERY, DADY	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,028	SHAEFFER ET AL.	
	Examiner	Art Unit	
	DADY CHERY	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/12/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/12/2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,5-7,13,14and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Baba et al. (US Patent 6,278,755, hereinafter Baba).

Regarding claim 1, Baba discloses a circuit **(Fig. 2)** for multiplexing a plurality of data signals **(30)** into an output data stream comprising:

a plurality of circuit elements **(43,45,47,49,etc),** wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal **(38)**

received from a source **(31)** other than one of the plurality of circuit elements, wherein an output of each circuit element of said plurality of circuit elements comprises an individual **(32)**data signal of said plurality of data signals and wherein said first clock signal is substantially in-phase with said transition**(Col. 8, lines 3 - 32);**

and a selector **(35)** coupled to said plurality of circuit elements for receiving each of the individual output data signals from the plurality of circuit elements and for sequentially selecting each of said individual data signals to generate said output data stream**(32),** wherein said selector is clocked to control said selecting by a second clock signal **(33)** received from a source other than one the plurality of circuit elements, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed offset **(Col. 8, lines 23- 57).**

Regarding claims 5 and 18, Baba discloses the circuit as recited in claim 1 further comprising a clock generator (**Fig. 2,31)** coupled to said selector**(35)** for generating said fixed offset **(Col. 8, lines 3 - 57);**

Regarding claims 6 and 19, Baba discloses the circuit as recited in claim 5 wherein said clock generator comprises a coupled oscillator circuit **(Fig. 2, 34 Col. 8, lines 3-57).**

Regarding claims 7, 20, Baba discloses the circuit as recited in claim 5 wherein said clock generator comprises a divide-by-two circuit **(Fig. 4, 50, Col. 10, lines 38 -50).**

Regarding claim 13 , Baba discloses *the circuit wherein a part of said plurality of circuit elements comprises a flip-flop* **(Fig. 2, 36).**

Regarding claim 14, Baba discloses in a circuit **(Fig. 2)** comprising a plurality of circuit elements **(43, 45, 47, 49, etc),** for providing a data signal with transitions in response to a clock signal and a selector coupled to said plurality of circuit elements for selecting said data signal for an output data stream, a method for multiplexing a plurality of said data signals into an output data stream **(Col. 8, lines 3 - 32);** comprising:

providing first and second clock signals received from a source **(31)** other than one of the plurality of circuits elements, wherein said second clock signal is out-of-phase with respect to said first clock signal by a fixed offset**(Col. 8, lines 3 - 32);**;

clocking said circuit elements with said first clock signal to control said transitions of said data signal Clocking said selector with said second clock to sequentially select a plurality of said data signals for said output data stream **(Col. 8, lines 23- 57).**

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2- 4, 15-17 and 25 -27and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Chen.

Regarding claim 25, Baba discloses a circuit **(Fig. 2)** for multiplexing a plurality of data signals **(30)** into an output data stream comprising:

a plurality of circuit elements **(43,45,47,49,etc),** wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal **(38)** received from a source **(31)** other than one of the plurality of circuit elements, wherein an output of each circuit element of said plurality of circuit elements comprises an individual **(32)**data signal of said plurality of data signals and wherein said first clock signal is substantially in-phase with said transition**(Col. 8, lines 3 - 32);**

and a selector **(35)** coupled to said plurality of circuit elements for receiving each of the individual output data signals from the plurality of circuit elements and for sequentially selecting each of said individual data signals to generate said output data stream**(32),** wherein said selector is clocked to control said selecting by a second clock signal **(33)** received from a source other than one the plurality of circuit elements, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed offset **(Col. 8, lines 23- 57).**

Baba does not explicitly discloses a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through said compensator, wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay.

However, Chen teaches a compensator **(14)** coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through

said compensator, wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay **(Col. 5, lines 1- 35).**

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Chen such a compensator into the teaching of Baba for the purpose of recovery the clock circuit **(Col. 4, lines 1- 9).**

Regarding claims 2, 15 and 26, Baba discloses all the limitation of claims 2,15 and 26, except the circuit as recited in claim 1 wherein said fixed offset comprises a quadrature offset. However, Chen discloses the circuit as recited in claim 1 wherein said fixed offset comprises a quadrature offset **(Col. 6, lines 11 -14, Lead and Lag output pulse).**

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Chen such a quadrature offset into the teaching of Baba for the purpose of recovery the clock circuit **(Col. 4, lines 1- 9).**

Regarding claims 3 and 16, Baba discloses all the limitation of claims 3 and 16, except the circuit as recited in claim 1 wherein said fixed offset comprises a delay. However, Chen teaches the circuit as recited in claim 1 wherein said fixed offset comprises a delay **(Col. 6, lines 11 -14, Lag output pulse).**

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Chen such a quadrature offset into the teaching of Baba for the purpose of recovery the clock circuit **(Col. 4, lines 1-9).**

Regarding claims 4 and 17, Baba discloses all the limitation of claims 3 and 16, except the circuit as recited in claim 3 wherein said delay comprises a quadrature delay. However, Chen teaches the circuit as recited in claim 3 wherein said delay comprises a quadrature delay **(Col. 6, lines 11 -14, Lead and Lag output pulse).**

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Chen such a quadrature delay into the teaching of Baba for the purpose of recovery the clock circuit **(Col. 4, lines 1-9).**

Regarding claim 27, Baba discloses the circuit as recited in claim 5 wherein said clock generator comprises a divide-by-two circuit **(Fig. 4, 50, Col. 10, lines 38 -50).**

Regarding claim 30, Baba discloses *the circuit wherein a part of said plurality of circuit elements comprises a flip-flop* **(Fig. 2, 36).**

8. Claims 8-12, 21-24and 28 -29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Chen as applied above, and further in view of Song.

Regarding claims 8, 21, Baba discloses all the limitations of claims 8 and 21, except *the delay comprises a propagation delay*

However, Song teaches *the method said delay comprises a propagation delay* **(Abstract).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the propagation delay in order to adjust the phase difference between difference signals **(Abstract)**

Regarding claims 9, 22 and 29, Baba in combination of Chen discloses all the limitations of claims 9, 22 and 29, except *the circuit further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.*

However, Song teaches *the circuit further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay* **(Fig. 2A, Abstract and Col. 4, lines 10 –28).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the propagation delay in order to adjust the phase difference between difference signals **(Abstract)**

Regarding claim 10, Baba discloses all the limitations of claim 10, except *the circuit further comprising a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element,*

wherein said second clock signal is transmitted to said selector through said compensator.

However, Song teaches *the circuit further comprising a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through said compensator* **(Fig. 2A, Col. 5, lines 20 - 37).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method teaching by Song into the method taught by Chen for the purpose of compensation of other delays introduced within the signal delay circuit itself **(Abstract).**

Regarding claims 11 and 28, Baba in combination with Chen discloses all the limitation of claims 11 and 28, except *the circuit wherein said compensator retards said second clock signal to said selector by a compensating delay.*

However, Song teaches *the circuit wherein said compensator retards said second clock signal to said selector by a compensating delay* **(Col. 5, lines 25 – 31).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method teaching by Song into the method taught by Chen for the purpose of compensation of other delays introduced within the signal delay circuit itself **(Abstract).**

Regarding claim 12, Baba discloses all the limitations of claim 12, except *said compensating delay corresponds to say clock-to-data delay.*

However, Song teaches *wherein said compensating delay corresponds to say clock-to-data delay* **(Col. 5, lines 20 – 23).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method teaching by Song into the method taught by Chen for the purpose of compensation of other delays introduced within the signal delay circuit itself **(Abstract).**

Regarding claim 23, Baba discloses all the limitations of claim 23, except *the method further comprising the step of delaying said second clock signal by a compensating delay.*

However, Song teaches *the method further comprising the step of delaying said second clock signal by a compensating delay* **(Abstract).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method teaching by Song into the method taught by Chen for the purpose of compensation of other delays introduced within the signal delay circuit itself **(Abstract).**

Regarding claim 24, Baba discloses all the limitations of claim 24, except *the method wherein said compensating delay corresponds to a delay from said first clock signal to said transitions.*

However, Song teaches *the method wherein said compensating delay corresponds to a delay from said first clock signal to said transitions* **(abstract).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the method teaching by Song into the method taught by Chen for the purpose of compensation of other delays introduced within the signal delay circuit itself **(Abstract).**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DADY CHERY whose telephone number is (571)270-1207. The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dady Chery/
Examiner, Art Unit 2416

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2416